

Substitute for Form 1449/PTO

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INFORMATION DISCLOSURE

STATEMENT BY APPLICANT

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Sheet

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of

2

Application Number

09/955,537

Filing Date

September 17, 2001

First Named Inventor:

Manish Shah

Art Unit

2631


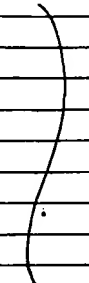

Examiner Name

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
Attorney Docket Number

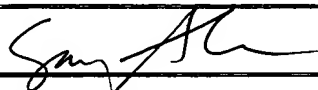
004259.P035

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		Number-Kind Code ² (If known)					
		US-	4,015,238	3/29/1977	Robert Curtis Davis	<div>RECEIVED</div> <div>AUG 1 1 2004</div> <div>Technology Center 2600</div>	
		US-	5,027,374	6/25/1991	Mark W. Rossman		
		US-	5,291,499 A	3/1/1994	Behrens et al.		
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		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
		WO	00/74264	A1	12/7/2000	Martone, Massimiliano		
		WO	01/59937	A2	8/16/2001	Qualcomm Inc.		

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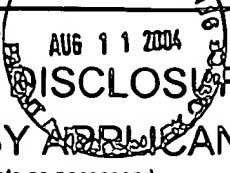
Date Considered

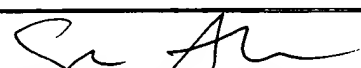
1/13/05

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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<div style="display: flex; justify-content: space-between; align-items: center;"> <div> <p>Substitute for Form 1449/PTO</p> <p>INFORMATION DISCLOSURE</p> <p>STATEMENT BY APPLICANT</p> <p><i>(use as many sheets as necessary)</i></p> </div> <div style="text-align: center;">  </div> </div>				<p>Complete if Known</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>Application Number</td> <td>09/955,537</td> </tr> <tr> <td>Filing Date</td> <td>September 17, 2004</td> </tr> <tr> <td>First Named Inventor:</td> <td>Manish Shah</td> </tr> <tr> <td>Art Unit</td> <td>2631</td> </tr> <tr> <td>Examiner Name</td> <td>Not Yet Assigned</td> </tr> <tr> <td>Attorney Docket Number</td> <td>004259.P03</td> </tr> </table>		Application Number	09/955,537	Filing Date	September 17, 2004	First Named Inventor:	Manish Shah	Art Unit	2631	Examiner Name	Not Yet Assigned	Attorney Docket Number	004259.P03
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Sheet	2	of	2	<p>AUG 11 2004</p> <p>Technology Center 2600</p>													
<p>NON PATENT LITERATURE DOCUMENTS</p>																	
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²												
[Signature]		BREE, ET AL., "A Bit-Serial Architecture For A VLSI Viterbi Processor", Communications Systems Research Group, University of Saskatchewan, Saskatoon, IEEE, WESCANEX '88, 1988, pages 72-77.															
[Signature]		BIVER, ET AL., "Architectural Design and Realization Of A Single-Chip Viterbi Decoder", Elsevier Science Publishers B.V., INTEGRATION, The VLSI Journal 8 (1989), October, No. 1, Amsterdam, NL, Pages 3-16.															
[Signature]		BREE, ET AL., "A Modular Bit-Serial Architecture For Large Constraint-Length Viterbi Decoding", Communications Systems Research Group, University of Saskatchewan, Saskatoon, Canada, IEEE International Conference on Communications", 1990, pages 1501-1506.															
[Signature]		CHOI, ET AL., "Viterbi Detector Architecture For High-Speed Optical Storage", 1997, IEEE TENCON - Speech and Image Technologies for Computing and Telecommunications, ASIC Center Corporate Technical Operations SAMSUNG Electronics, Vol. 1, Dec 1997, pages 89-92.															
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[Signature]		HASHIDA MITSUYOSHI, "Hierarchical Network Management System and Control Method for Network Management Information," Patent Abstracts of Japan, Publication No. 07226777															

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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 04259.P035	Application Number: 09/955,537
	First Named Inventor: Manish Shah	
	Filing Date: September 17, 2001	



U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Code ²	Kind (If known)			
<i>sw</i>		5,778,192		Schuster, et al.	7-7-1998	
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		Office ³ Code ⁵	Number ⁴	Kind (If known)				
<i>a</i>		EP	0 762 777		Uchiumi, Tadasgu, et al.	3-12-1997		

Examiner Signature	<i>Jim Allen</i>	Date Considered	1/13/05
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 04259.P035	Application Number: 09/955,537
	First Named Inventor: Manish Shah, et al.	<div style="text-align: center;"> RECEIVED MAR 08 2002 Technology Center 2600 </div>
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		Number	Kind Code ² (If known)			
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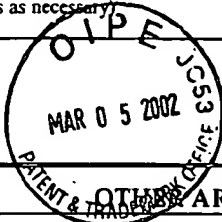

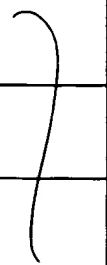

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OTHER ART - NO PATENT LITERATURE DOCUMENTS Technology Center 2600			
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		JOHN G. PROAKIS, Block and Convolutional Channel Codes, Digital Communications, Fourth Edition, Pages 416 - 547, McGraw-Hill Series in Electrical and Computer Engineering, New York, NY.	
		"www.inventra.com/inventra/softcore/workshop/MultiRaFiltDes95/" MENTOR GRAPHICS, Hardware Design of Decimators/Interpolators, Pages 1-38.	
		"www.mentor.com/inventra/softcore/workshop/SDmod95/", MENTOR GRAPHICS, Introduction to AD/DA Converters, Pages 1-27.	
		http://www.mentor.com/inventra/softcore/workshop/SDHWDes95/ MENTOR GRAPHICS, Design of the Decimation & Interpolation Filters, Pages 1-57.	
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